ABSTRACT

An debug and emulation system includes a target device embodied in a single integrated circuit. The target device includes a function clock circuit and an operation circuit operating in synchronism with the function clock. A trace trigger circuit triggers trace operation upon detection of a predetermined condition within the operation circuit. A FIFO buffer receives the trace data which is exported via a trace port. The integrated circuit includes an oscillator clock circuit which may be synchronized with the function clock or a reference clock. The trace trigger circuit and the FIFO input operate on the function clock. The FIFO output and the trace port operate on the oscillator clock. Thus the trace may operate all on the function clock or be split between the function clock and the reference clock. The trace data is sensed in synchronism with the oscillator clock. The emulator is coupled to the target device to control the clock selection. Accordingly, the trace export can operate at a frequency independent of the operation circuit.